

FIG. 1A

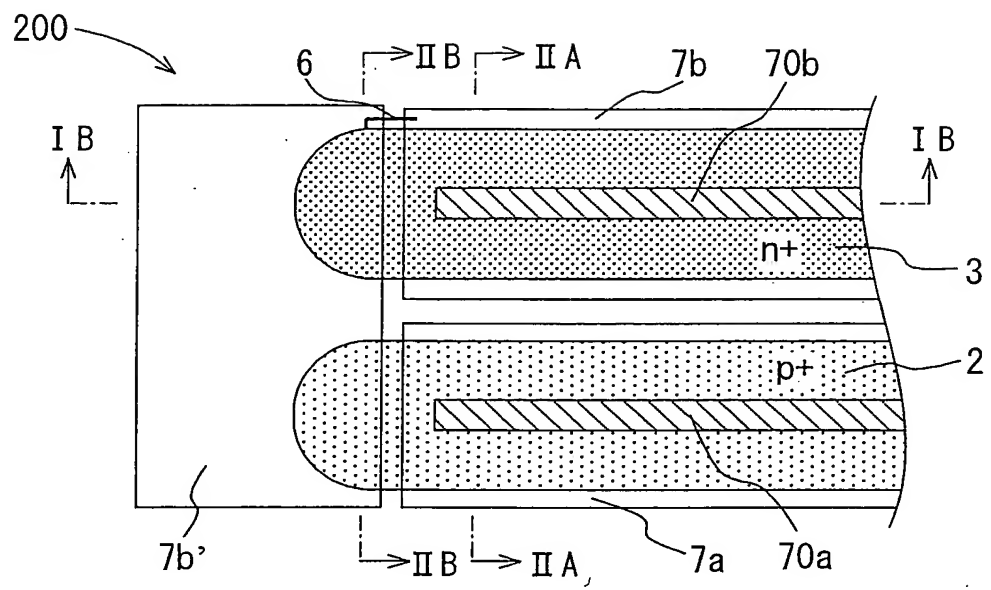


FIG. 1B

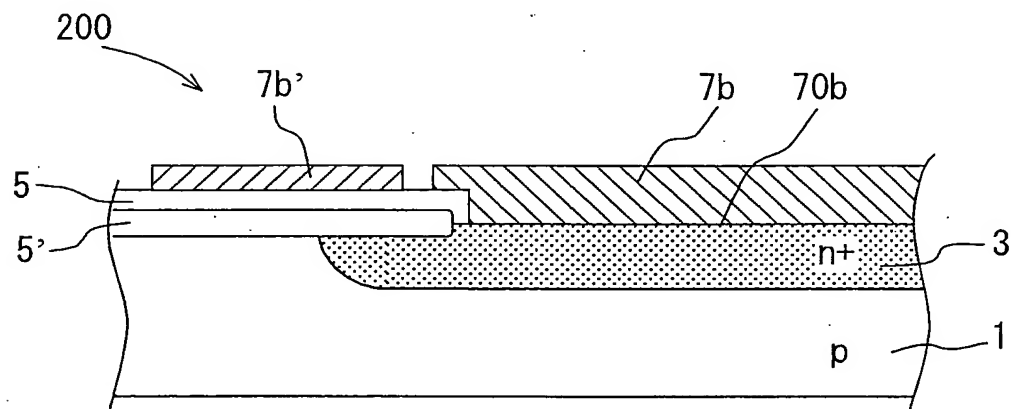


FIG. 2A

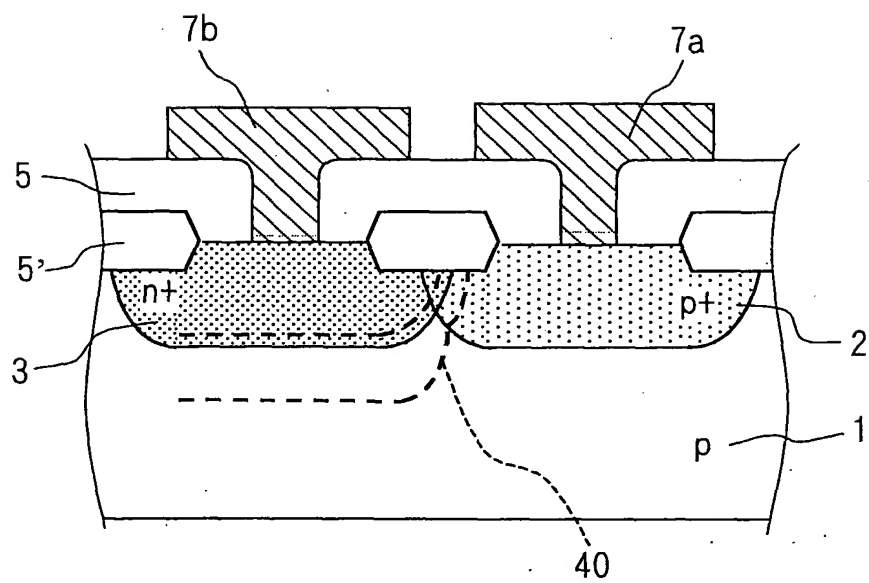


FIG. 2B

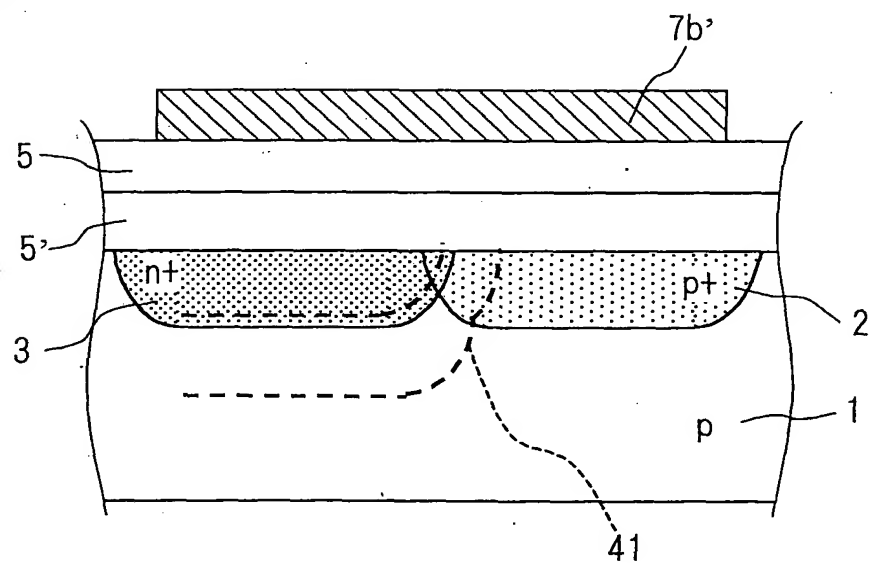


FIG. 3A

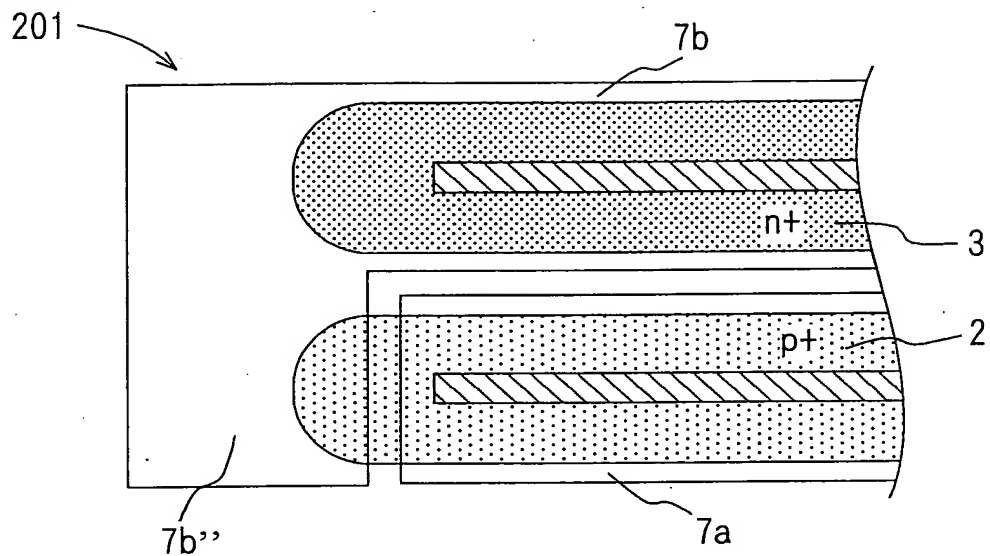


FIG. 3B

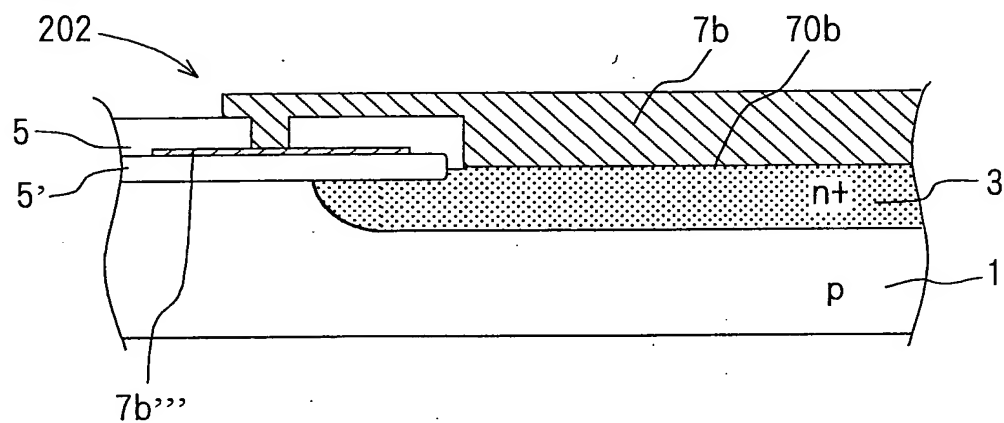


FIG. 4

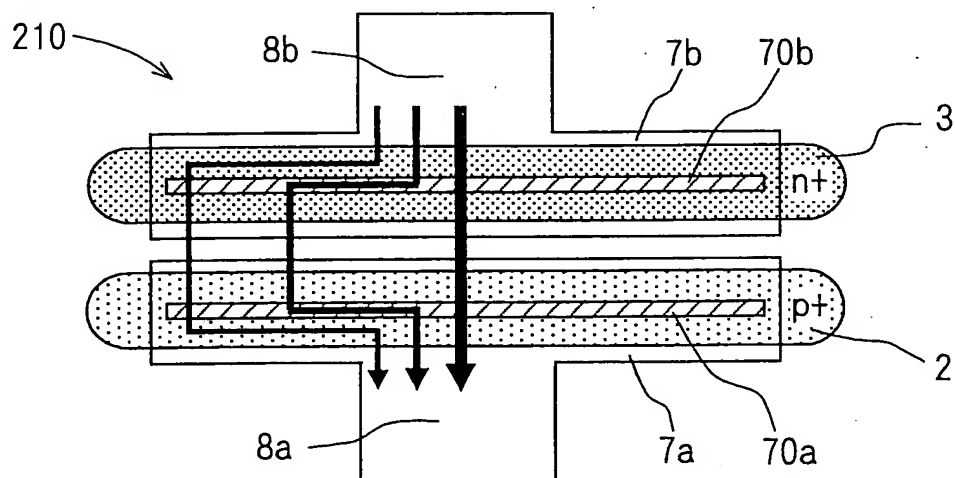


FIG. 5

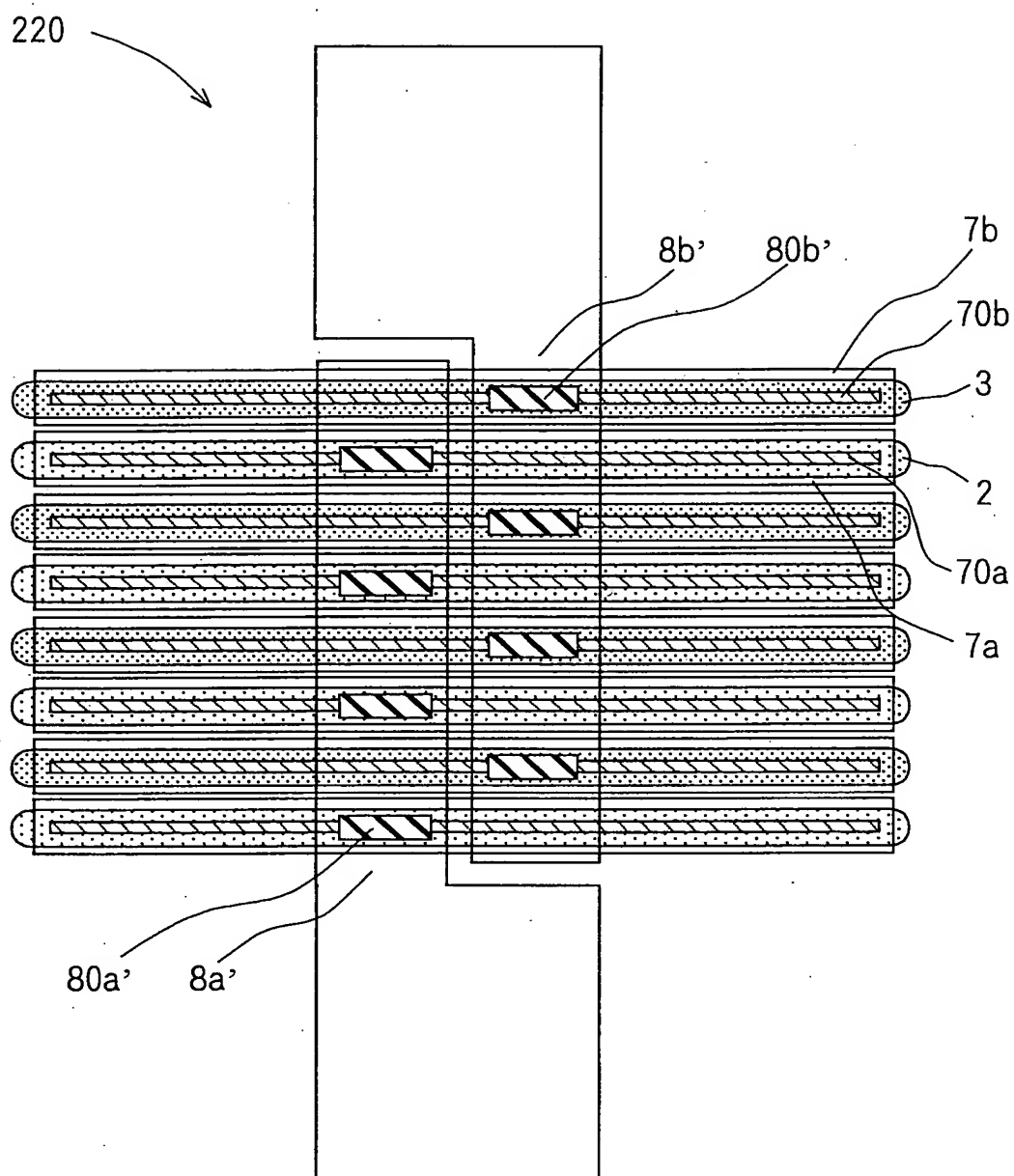
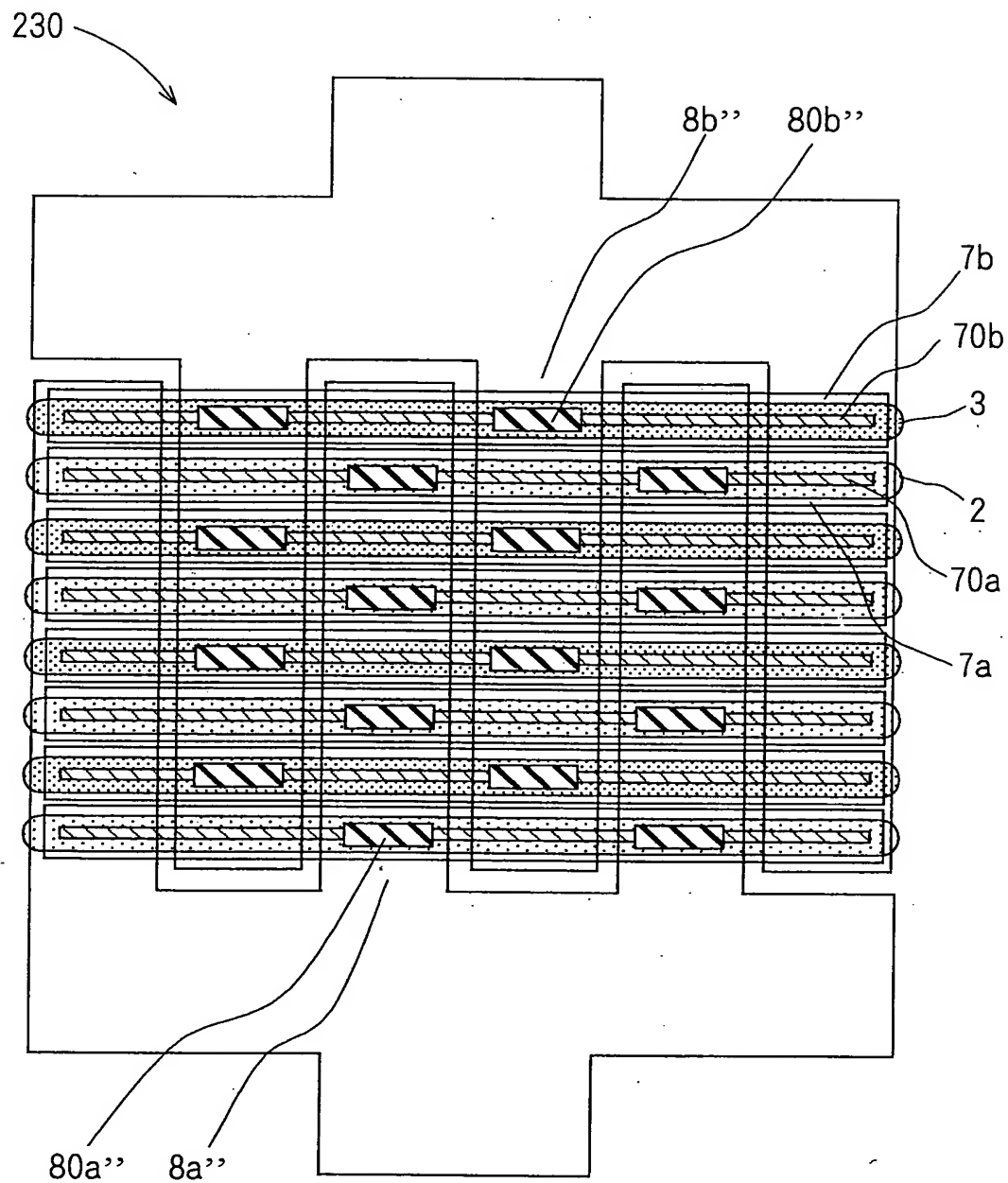


FIG. 6



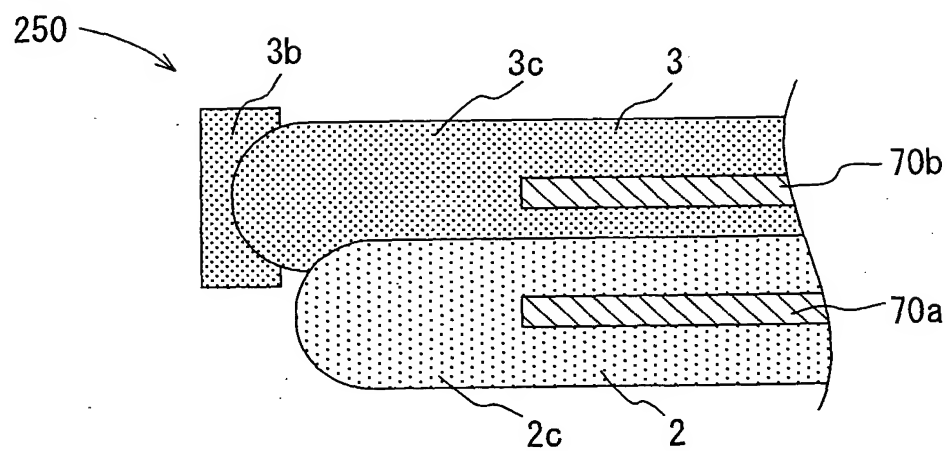


FIG. 9A

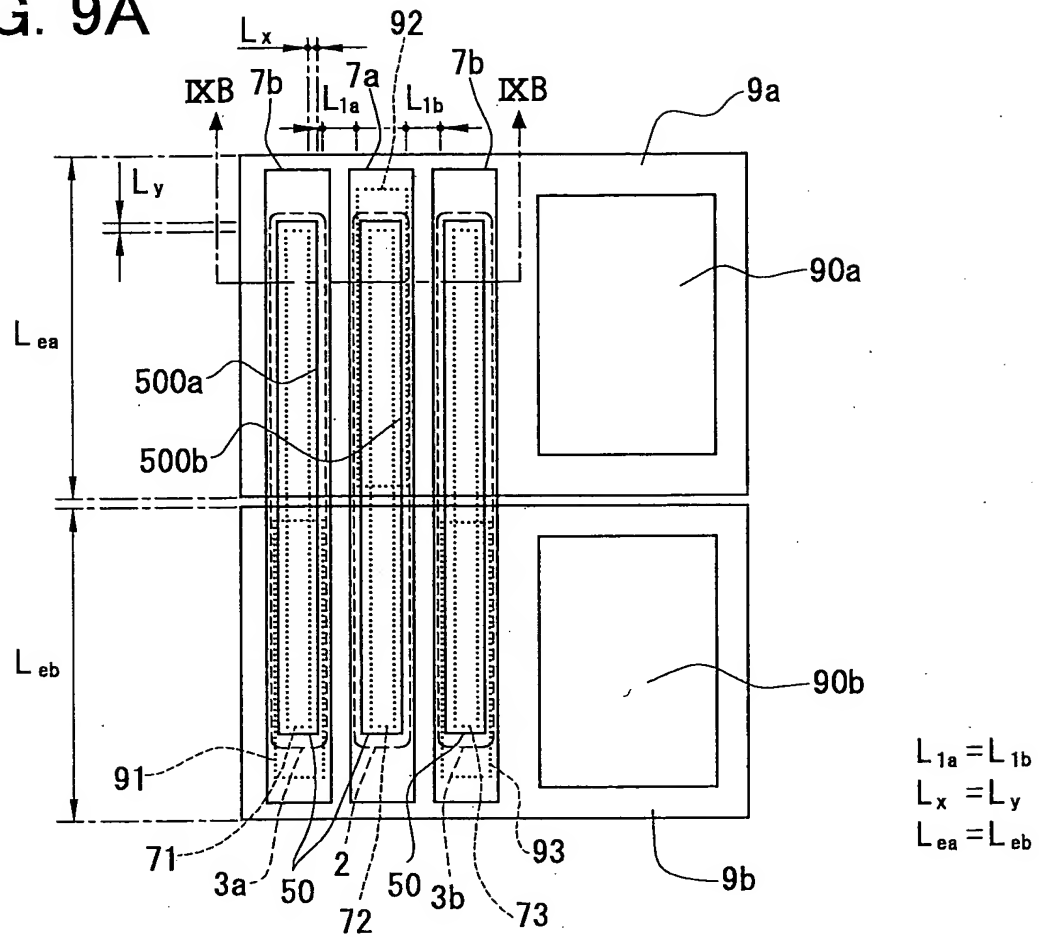


FIG. 9B

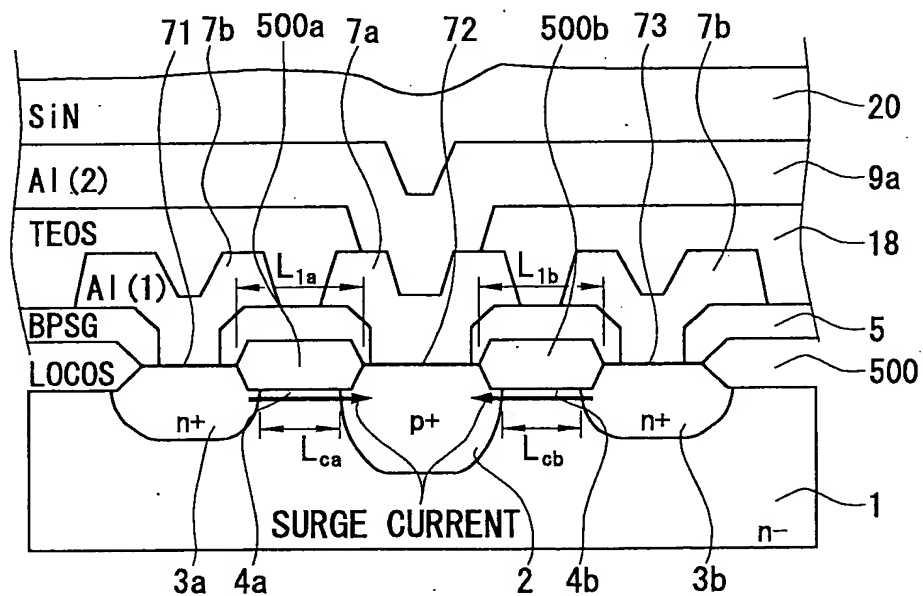


FIG. 10A

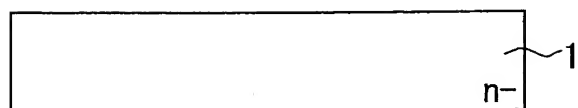


FIG. 10B

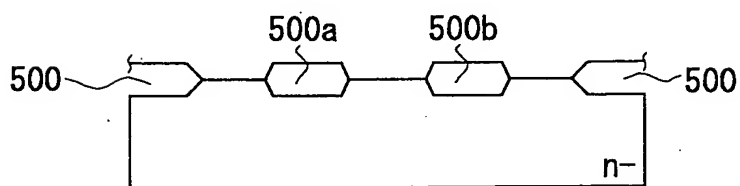


FIG. 10C

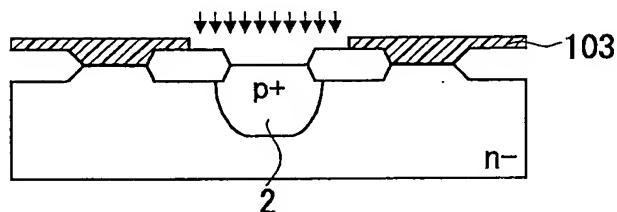


FIG. 10D

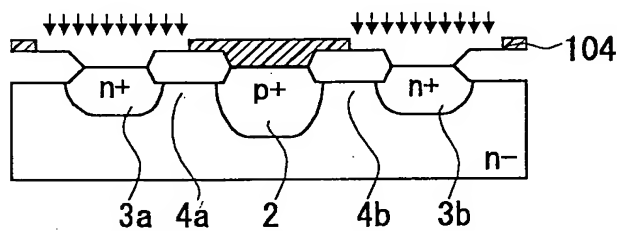


FIG. 10E

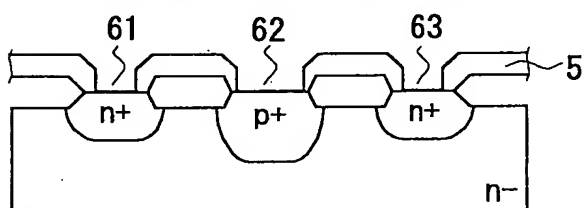


FIG. 10F

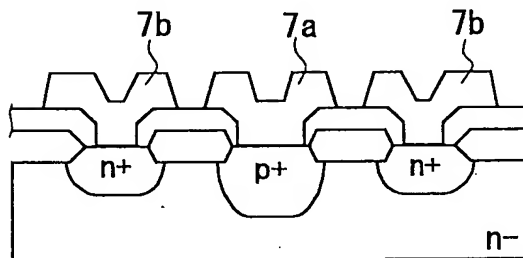


FIG. 10G

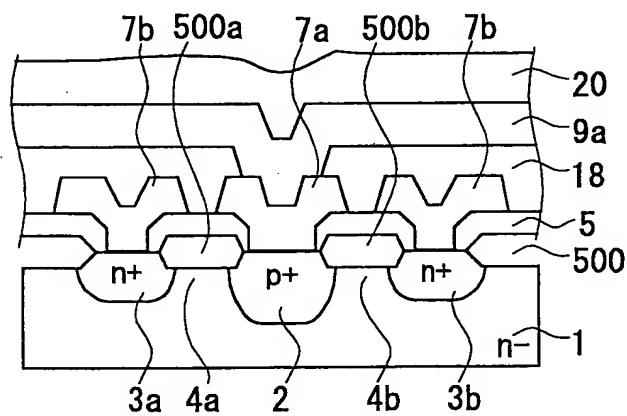


FIG. 11A

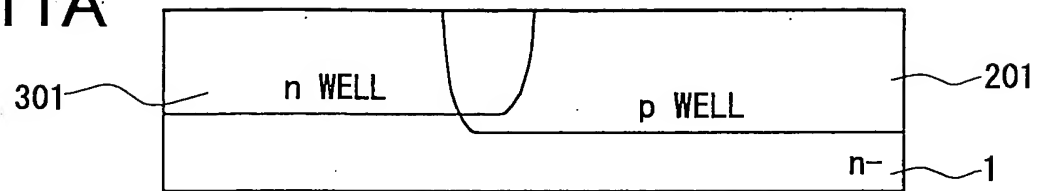


FIG. 11B

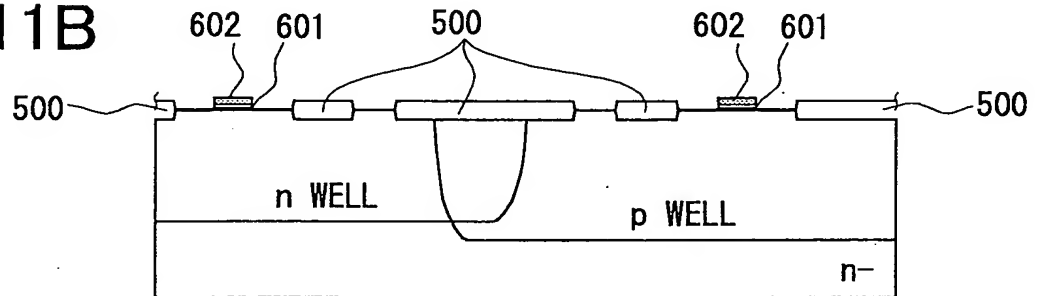


FIG. 11C

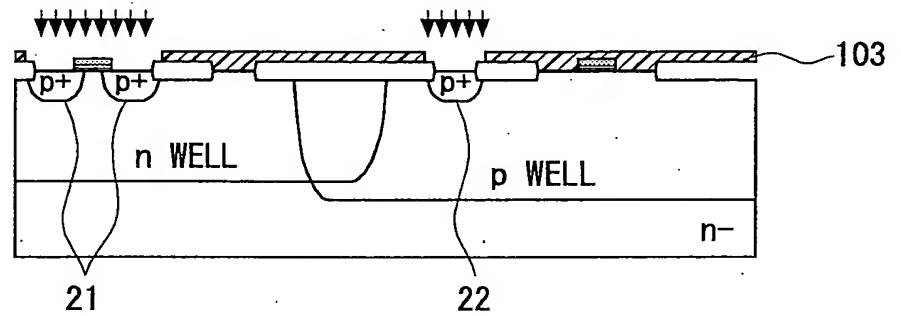


FIG. 11D

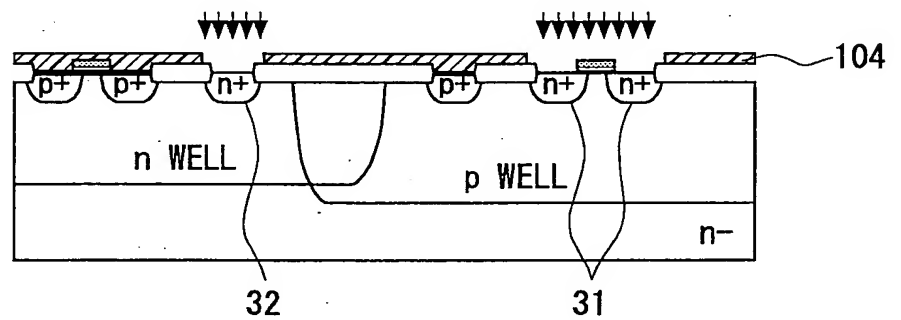


FIG. 11E

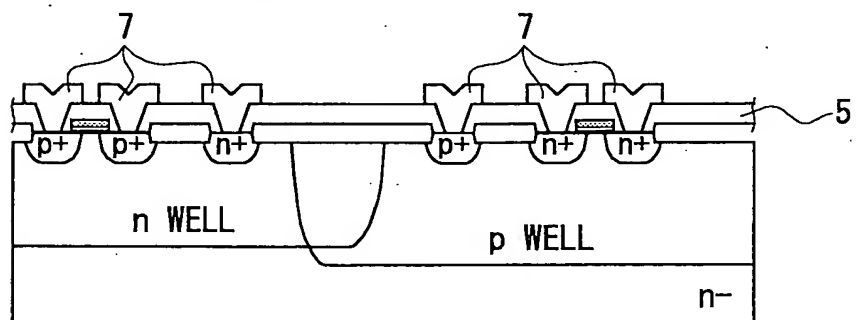


FIG. 12

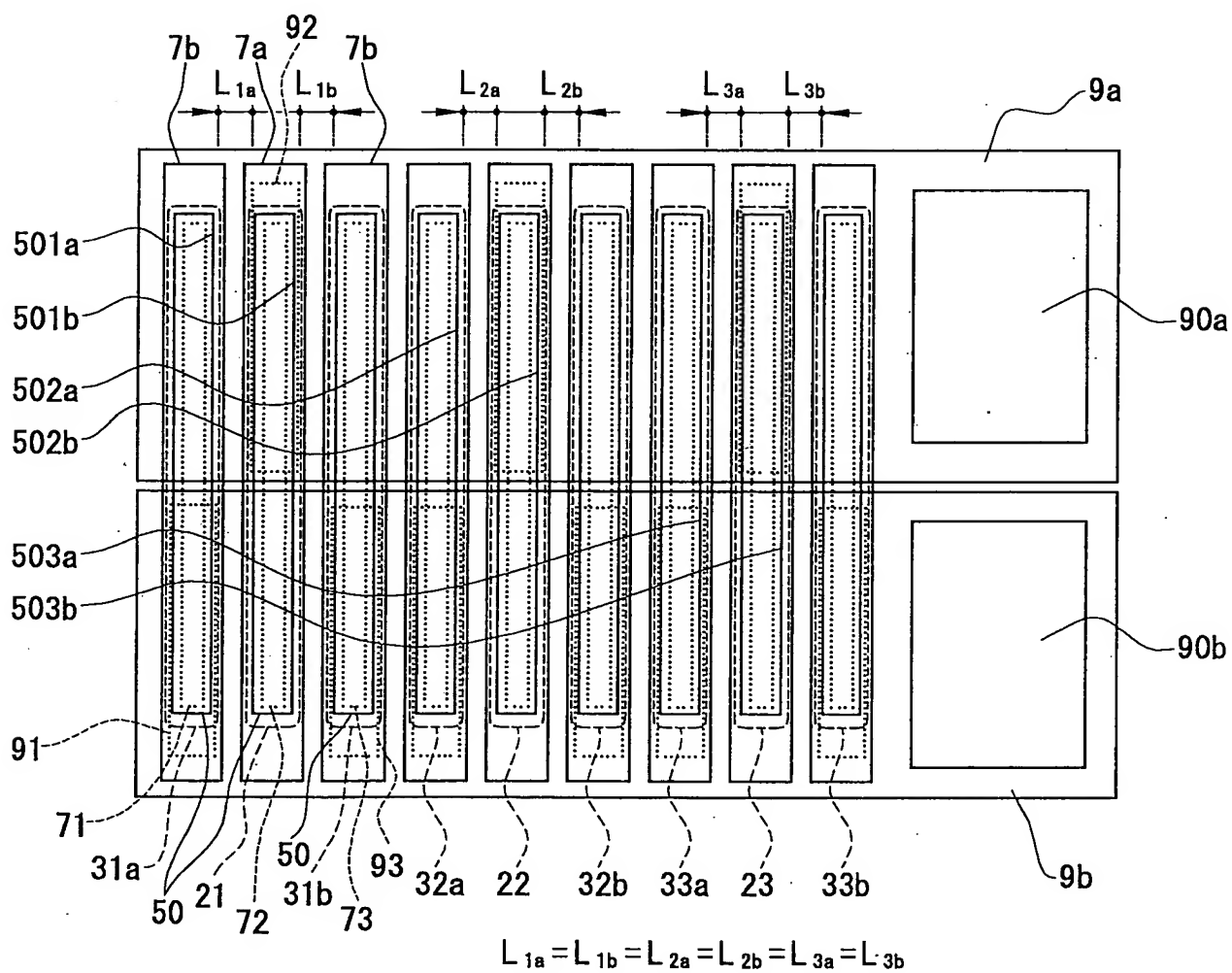


FIG. 13

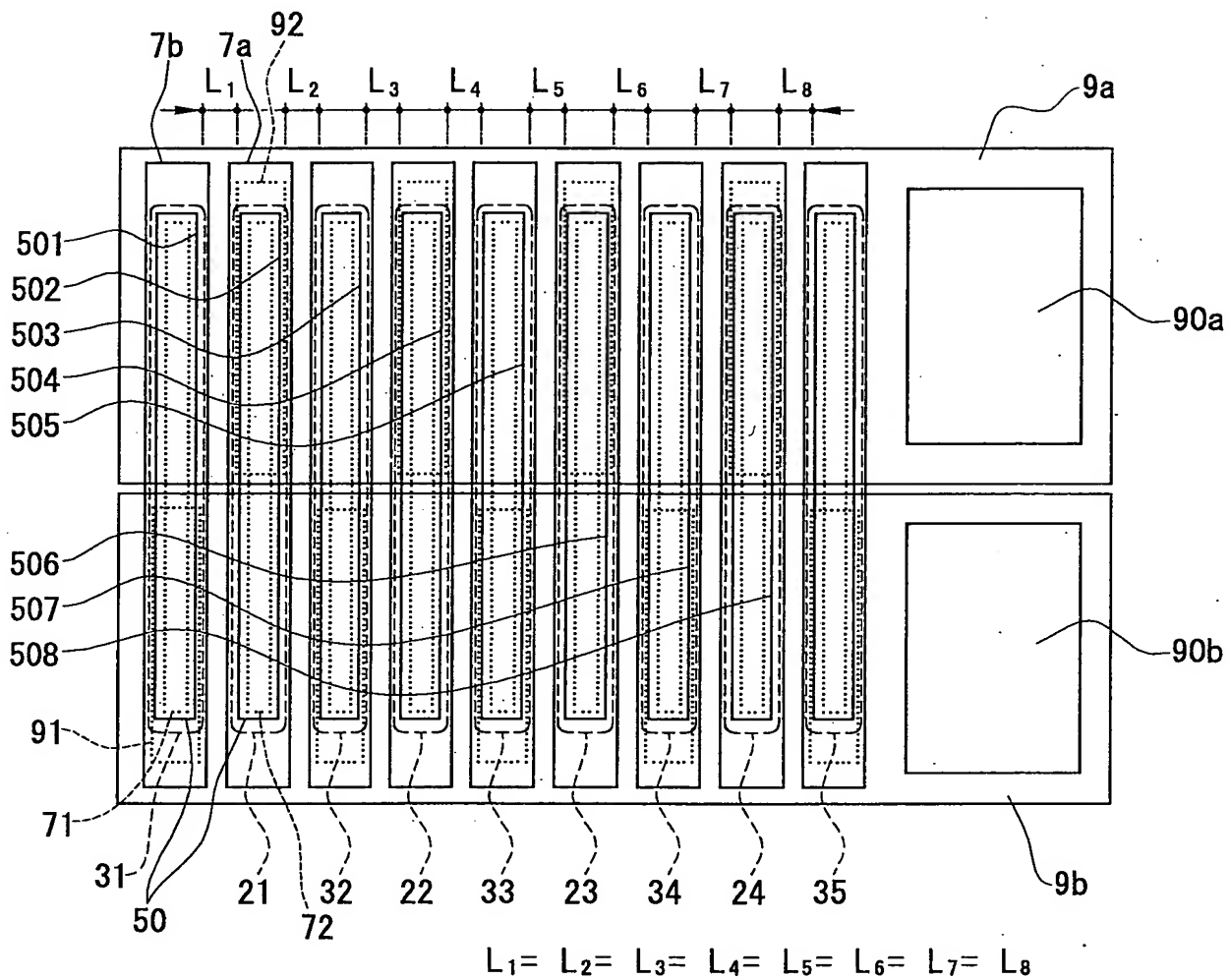


Figure 1 is a schematic diagram of a multi-layer printed circuit board (PCB) layout. The diagram shows a rectangular board divided into two horizontal sections, 90a (top) and 90b (bottom), separated by a central horizontal line 9a. The board is populated with eight vertical strips of components, labeled 7a and 7b. Each strip contains a series of rectangular components, with labels 501 through 508 indicating specific components. The strips are connected to a common ground plane 91. Dimensions are indicated: L_1 through L_8 for the width of each strip, and L_p and L_n for the height of the top and bottom sections respectively. The diagram also shows various other components and connections, including 31, 21, 32, 22, 33, 23, 34, 24, 35, 51, 52, 53, 54, 55, 56, 57, 58, 59, 71, and 92.

FIG. 15

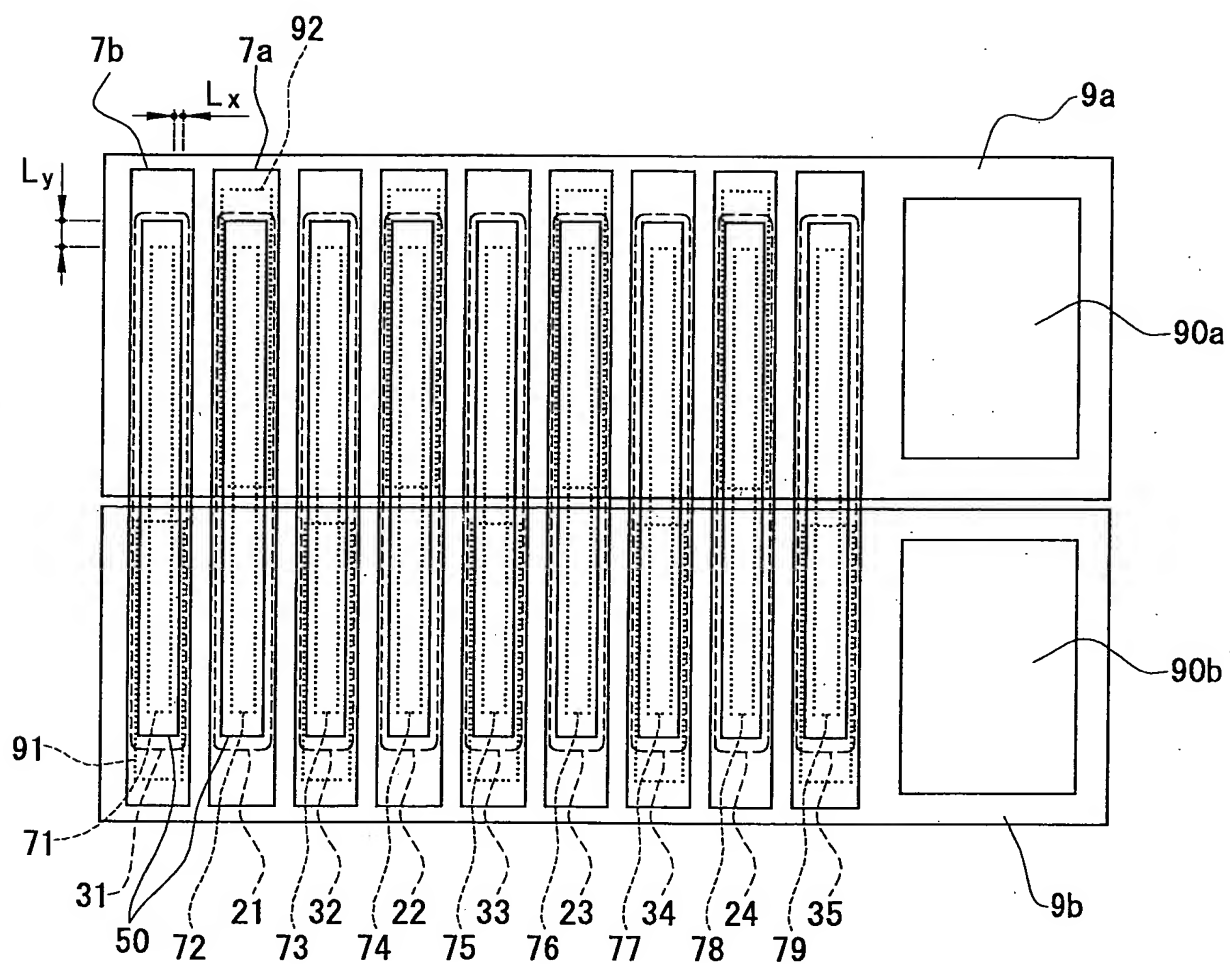


FIG. 16

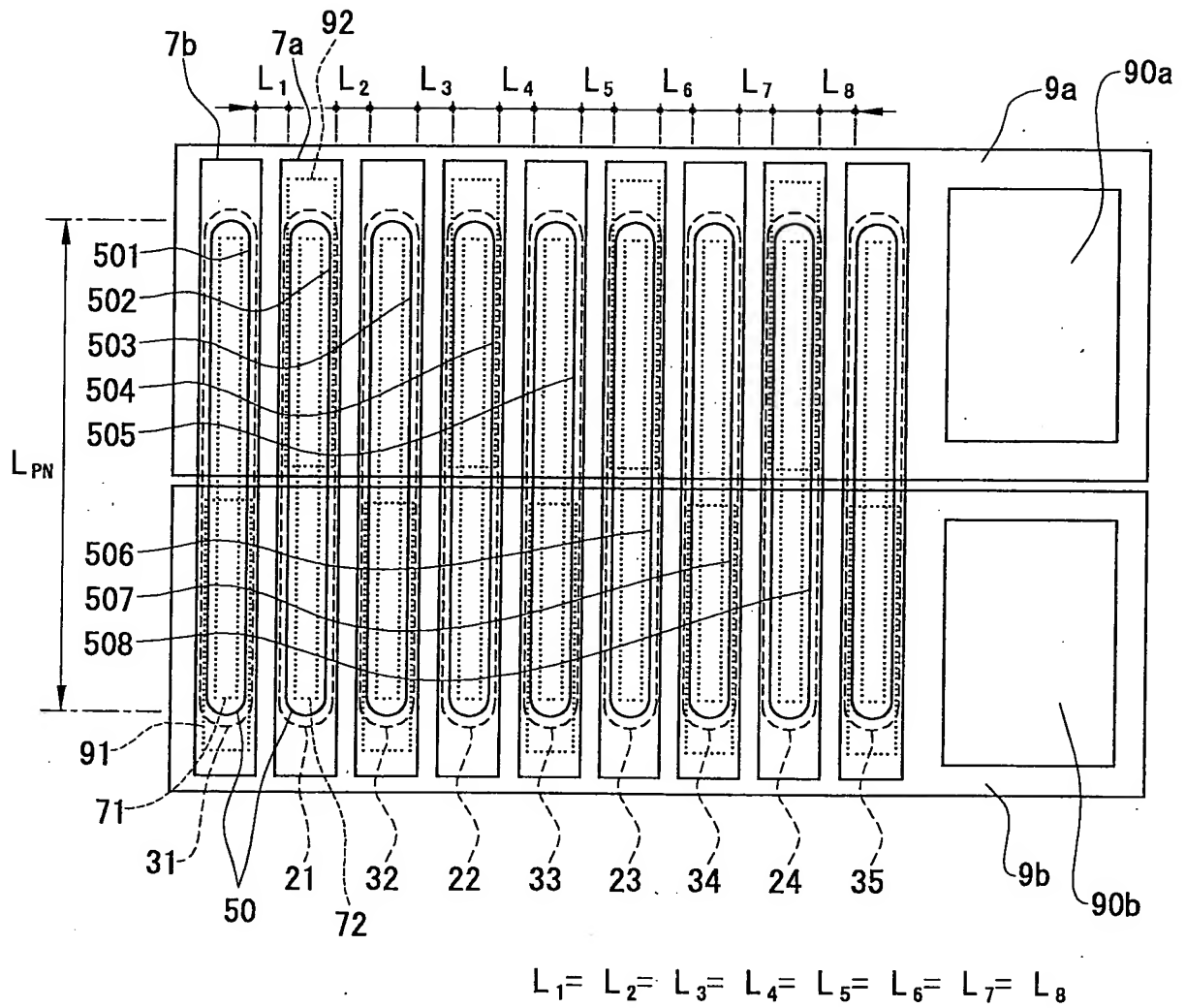


FIG. 17A

FIG. 17A is a detailed schematic diagram of a multi-layered printed circuit board (PCB) layout. The diagram shows a grid of vertical strips (302, 304, 306, 308, 310) and horizontal strips (71, 72, 73, 74, 75, 76, 77, 78, 79, 80). The strips are labeled with various reference numerals (e.g., 302, 304, 306, 308, 310, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80) and dimensions (L₁, L₂, L₃, L₄, L₅, L₆, L₇, L₈, L_p, L_n). The layout is divided into two main sections, 9a and 9b, by a horizontal line 78. The top section 9a contains a grid of vertical strips and horizontal strips, while the bottom section 9b contains a grid of vertical strips and horizontal strips. The strips are labeled with various reference numerals (e.g., 302, 304, 306, 308, 310, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80) and dimensions (L₁, L₂, L₃, L₄, L₅, L₆, L₇, L₈, L_p, L_n). The layout is divided into two main sections, 9a and 9b, by a horizontal line 78. The top section 9a contains a grid of vertical strips and horizontal strips, while the bottom section 9b contains a grid of vertical strips and horizontal strips. The strips are labeled with various reference numerals (e.g., 302, 304, 306, 308, 310, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80) and dimensions (L₁, L₂, L₃, L₄, L₅, L₆, L₇, L₈, L_p, L_n).

FIG. 18

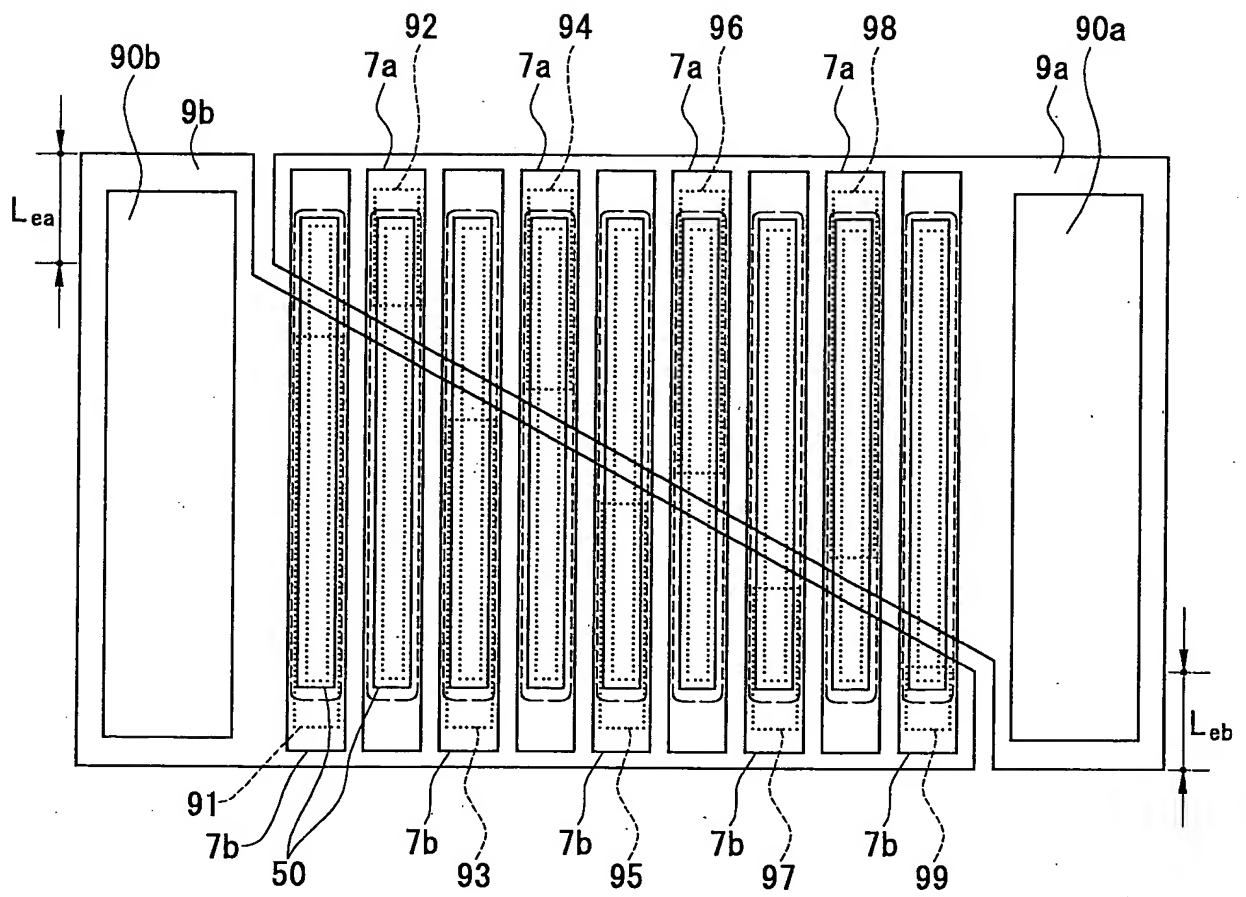


FIG. 19A

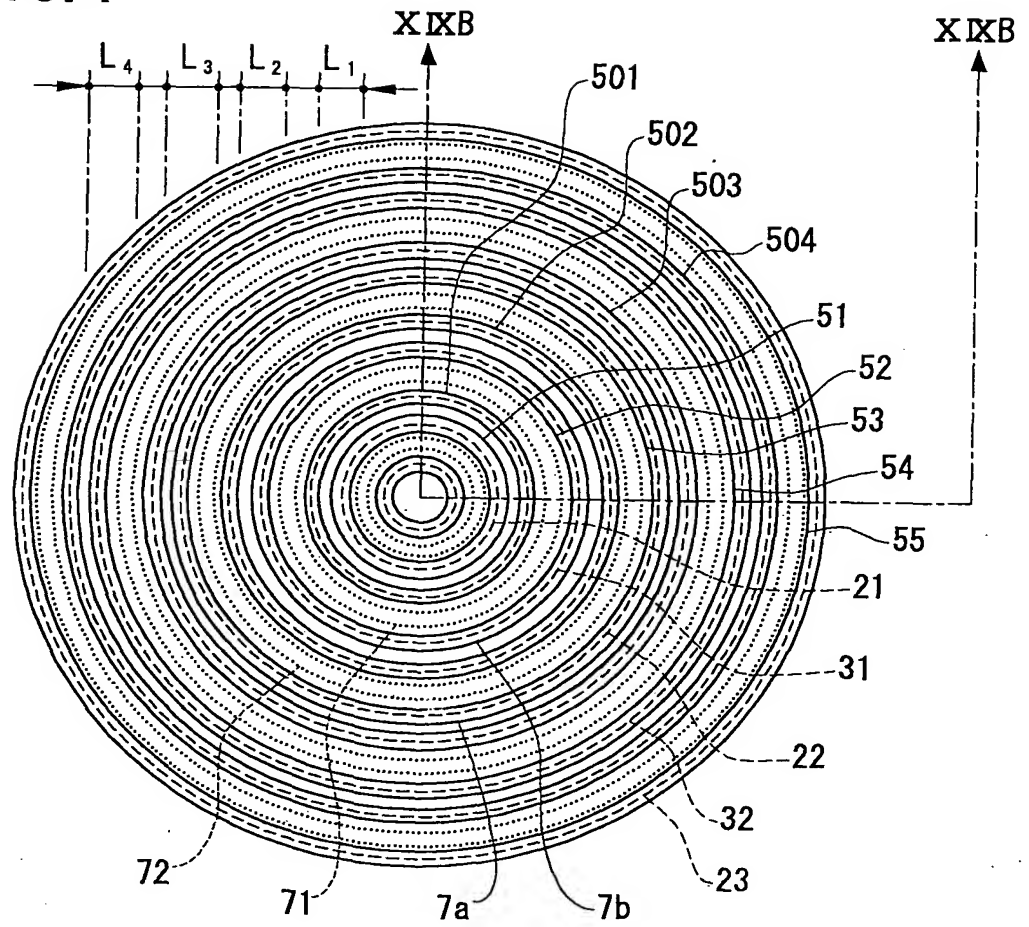


FIG. 19B

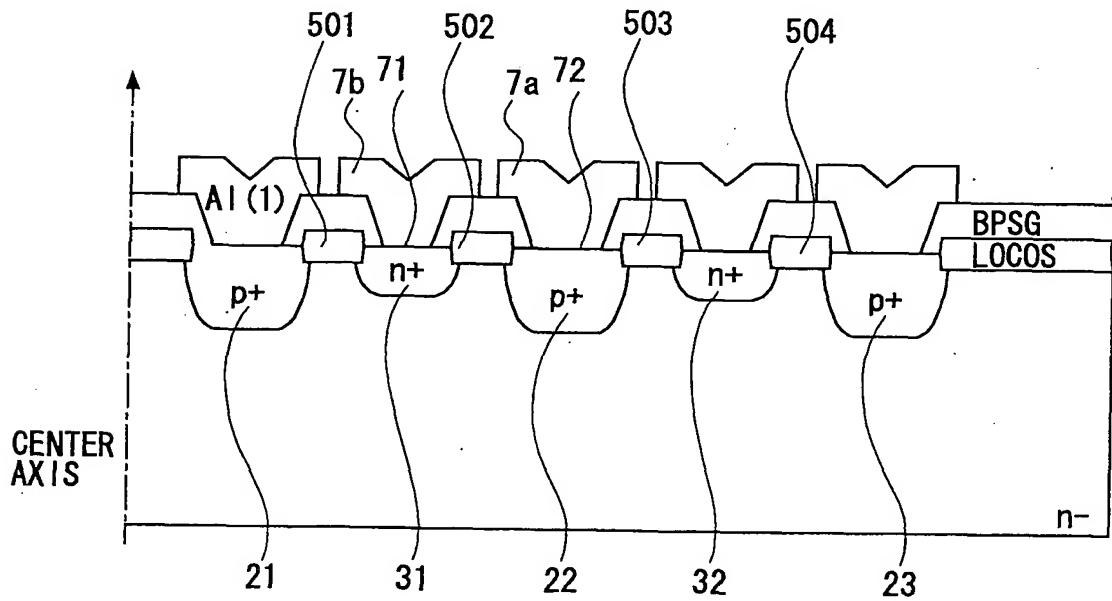


FIG. 20A

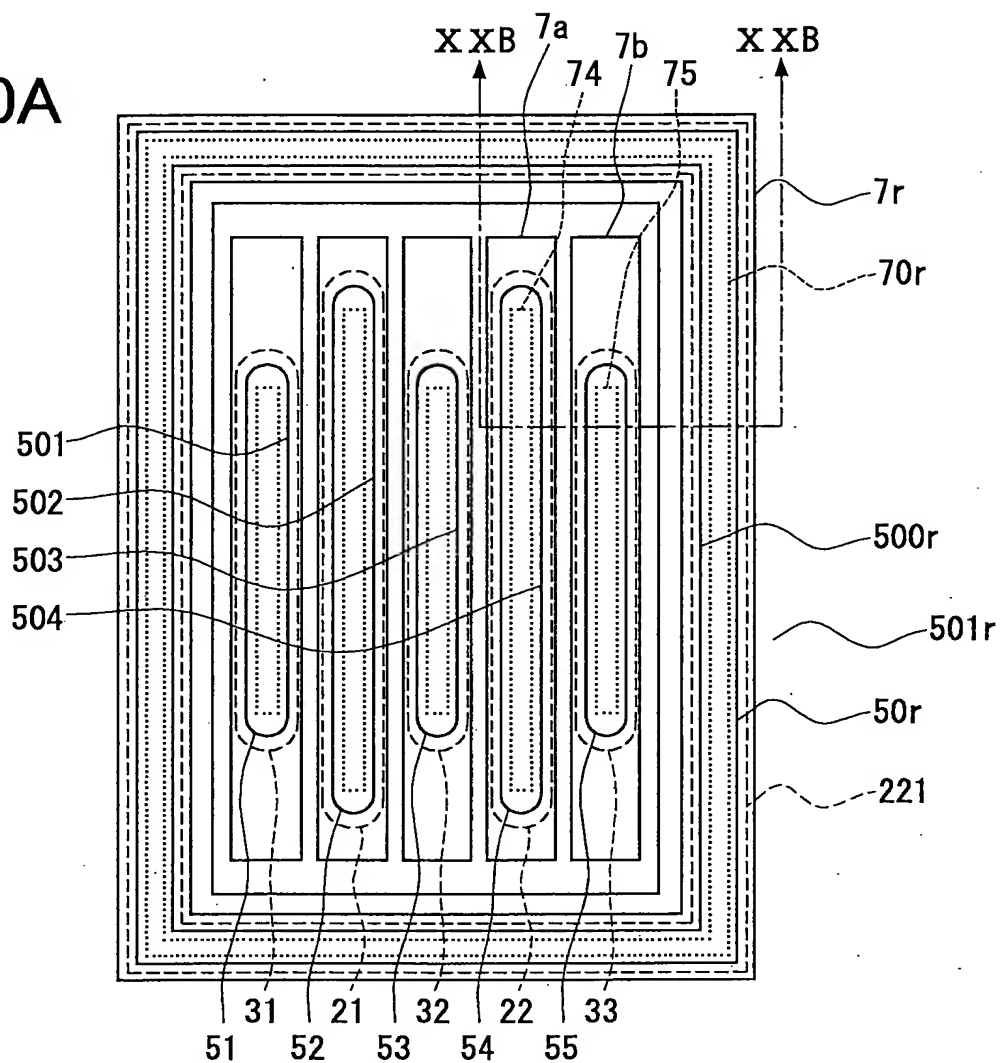
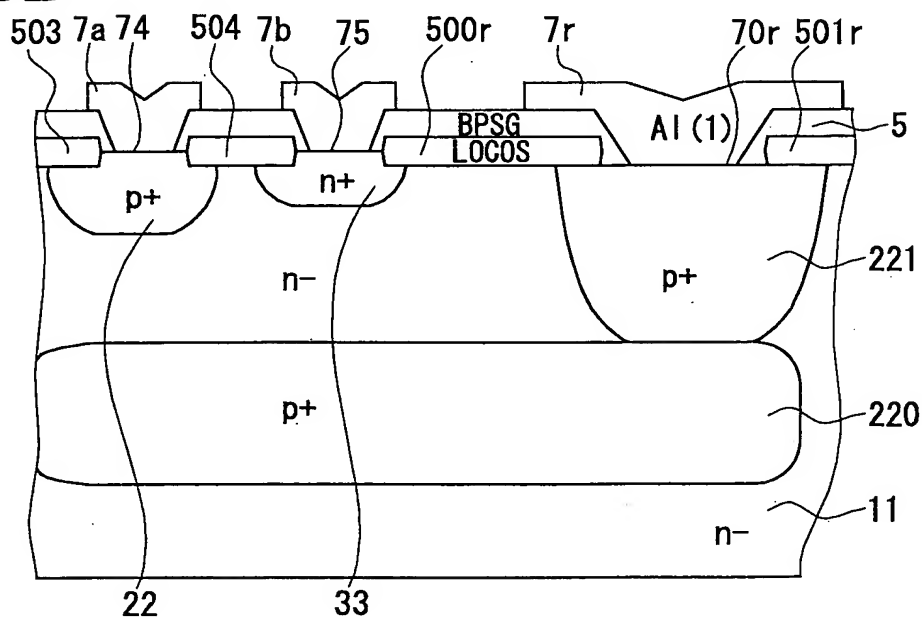


FIG. 20B



This cross-sectional view shows a semiconductor device with a gate stack on top. The gate stack includes a layer labeled **Al (1)** and a layer labeled **LOCOS**. The gate stack is divided into regions labeled **503**, **7a**, **74**, **504**, **7b**, **75**, and **500r**. Below the gate stack, there are **p+** and **n+** regions. The **p+** region is labeled **22** and the **n+** region is labeled **33**. To the right, there is a channel region with a **SiO2** layer and a **POLY Si** layer. The channel region is labeled **11** and **401**. The **SiO2** layer is labeled **700** and the **POLY Si** layer is labeled **402**. The channel region is also labeled **n-** at the bottom.

FIG. 22A
RELATED ART

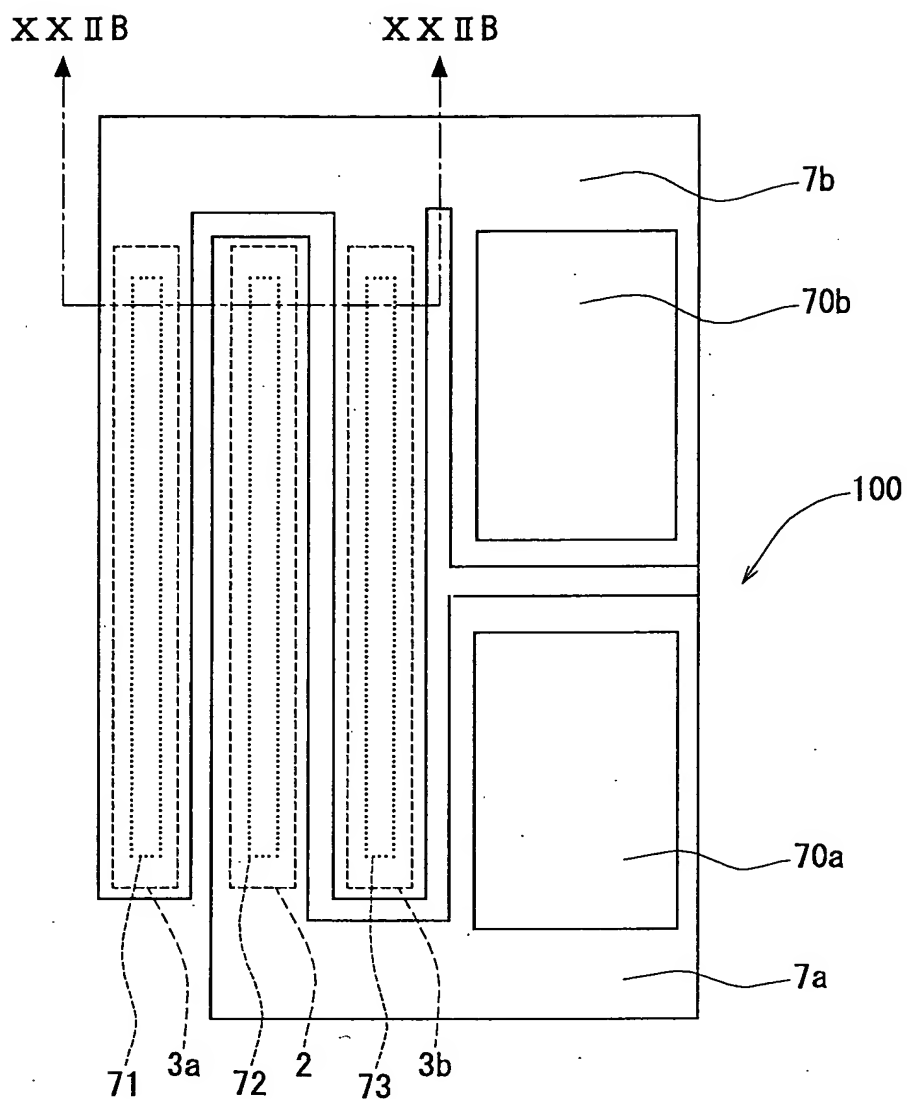


FIG. 22B
RELATED ART

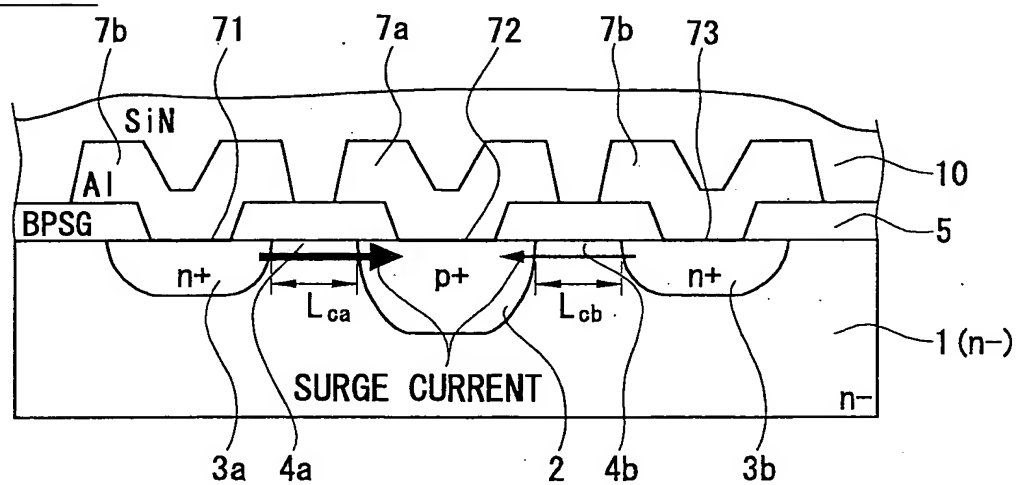


FIG. 23A
RELATED ART

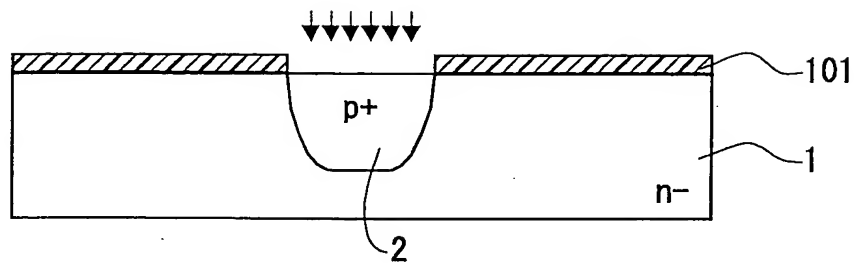


FIG. 23B
RELATED ART

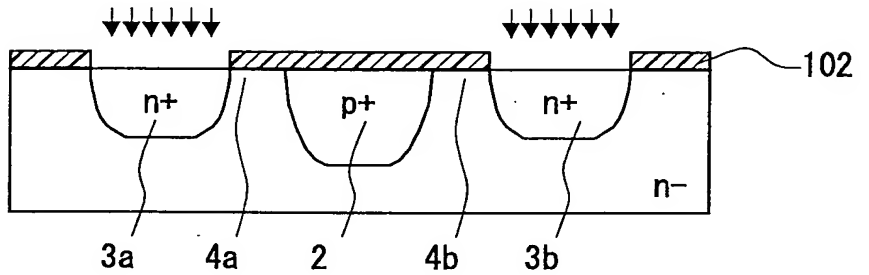


FIG. 23C
RELATED ART

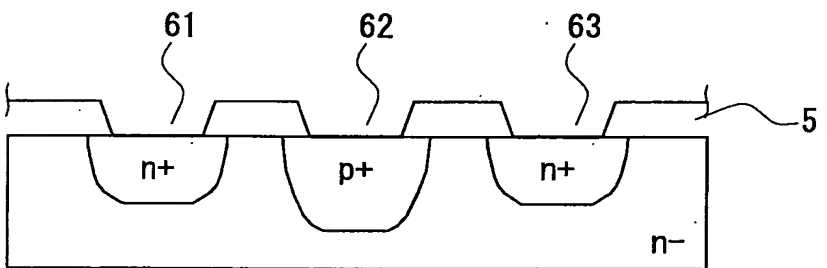


FIG. 23D
RELATED ART

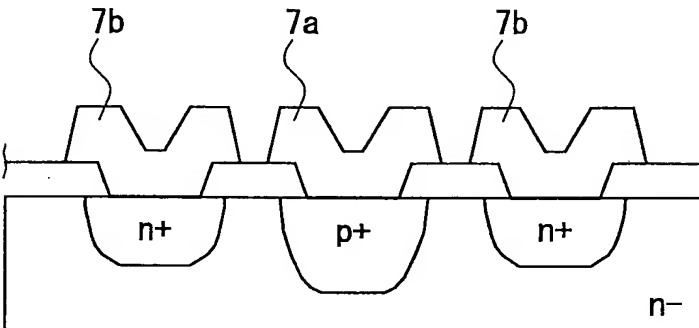


FIG. 23E
RELATED ART

